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Configuring the MAX3861 AGC Amp as an SFP Limiting Amplifier with RSSI

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1 Introduction

As optical transceiver modules decrease in size and increase in required features, demand for a compact limiting amplifier with Received Signal Strength Indicator (RSSI) continues to grow. Limiting amplifiers offer a low jitter data output, while RSSI, given TIA gain and photodiode responsivity, provides a method to monitor the optical input power. Both of these features are required in the Small Form-Factor Pluggable (SFP) multi-source agreement and in other applications.

The small 4mm x 4mm QFN package and on-chip RSSI of the MAX3861 make it an attractive postamp choice in SFP modules. The MAX3861 is a postamp with automatic gain control (AGC), which differs from a limiting amplifier. For reasons given in this discussion, an AGC amplifier may not be as attractive as a limiting amplifier for SFP modules. The purpose of this design note is to modify the MAX3861 post amplifier with automatic gain control to act as a limiting amplifier with RSSI.

2 Theory and Application of the MAX3861 and AGC Amplifiers

In general, automatic gain control amplifiers linearly amplify or attenuate the input signal while maintaining constant output amplitude. This is accomplished by a feedback loop. A power detector monitors the output amplitude and adjusts the gain of the variable amplifier stages in order to maintain a constant output voltage. Through continuous feedback, the signal is never limited and the output is therefore a linearly amplified version of the input.

Linear amplification is particularly useful in long-haul dense wavelength-division multiplexing (DWDM) systems that employ optical amplifiers. These optical amplifiers, typically erbium-doped fiber amplifiers, or EDFAs, induce more noise on a data high than on a data low. An AGC is particularly useful in this application, whereas a limiting amplifier is not. This is explained by the following example:

When an optical signal is detected by a photodiode-TIA with a limiting amplifier following it, the limiting amplifier makes the decision whether the data is a “1” or a “0”, by limiting the signal high or low. If noise is present on the 1 and the signal-to-noise ratio is sufficiently low, the noise on the 1 will occasionally drop below the decision threshold. If this happens, the limiting amplifier will output a 0, when the data is a 1. In contrast, using an AGC and operating in the linear region of the TIA maintains a linear signal path from the photodiode through the post amplifier. In this case, the next stage, usually a clock and data recovery (CDR) unit, can make the decision. On CDRs with vertical threshold adjust, the decision threshold can be adjusted below the noise to produce the optimal bit error rate (BER).

Linear amplifiers are not ideal for all systems, however. In an optical system without optical amplifiers, it is assumed that the same noise will be present on a 1 as on a 0. Limiting amplifiers are ideal for this situation because they produce faster output transition times, which decrease output jitter. In contrast, since an AGC is linear, its output transition times are based on the input transition times. In a 2.7Gbps module, the input transition time to the postamp can typically be in the range of 130ps-140ps (20%-80%), due to the bandwidth of the receiver, FR-4 stripline limitations, and other factors. In this case, the output transition time of an AGC amplifier will be about 140ps-150ps. This slow edge can result in increased jitter and therefore increased BER.

3 Opening the Gain Control Loop

To make the MAX3861 limit the input signal, the AGC loop needs to be opened and the gain set to the maximum. Referring to Figure 1, a differential voltage V_{CG} between CG+ and CG- of about 80mV sets the amplifier to its maximum gain of 43.5dB, which would give a $920mV_{P-P}$ output for an input of $6mV_{P-P}$.

3.1 Methods of Setting the Gain

The objective is to find a simple method to set the gain that can be implemented in a module or other small standalone setting.

It appears that the gain curve in Figure 1 saturates above V_{CG}=80mV, so any V_{CG} voltage (V_{CG+} - V_{CG-}) above 80mV should provide maximum gain in all conditions. Therefore, an easy solution would appear to be connecting CG+ to V_{CC} and CG- to ground, but this option is not recommended because these voltages may border on the absolute maximums given in the data sheet (V_{CC}-3.5V to V_{CC} + 0.5V). Another solution must be found.

Using the property that the CG pins are self-biasing to V_{CC}-1V, a resistor, R_{CG-}, can be connected from CG- to GND to set up a voltage divider inside the circuit, and let CG+ self-bias. If the CG- pin can be pulled low enough, at least 80mV below CG+, the amplifier will limit. As seen in Figure 2, the higher the resistance R_{CG-}, the more the amplifier behaves as an AGC, translating the input edge speeds to the output. This behavior is because the resistor loads the CG- pin less as resistance increases, and causes CG- to pull towards its self-biased state. With 138ps (20%-80%) input rise times, the optimal R_{CG-} value is about 800kΩ over the full V_{CC} range of 3.0V to 3.6V. Values down to about 100kΩ are permitted, but anything below that is not recommended. See Figure 3 for the test setup.

For a given V_{CG} (or, equivalently, R_{CG-}) in the limiting range and a given input above the sensitivity, the slew rate of the MAX3861 is constant. This implies that output transition times will be longer at larger output amplitudes. It should be noted that the numbers in Figure 2 are taken with V_{SC}=0V.

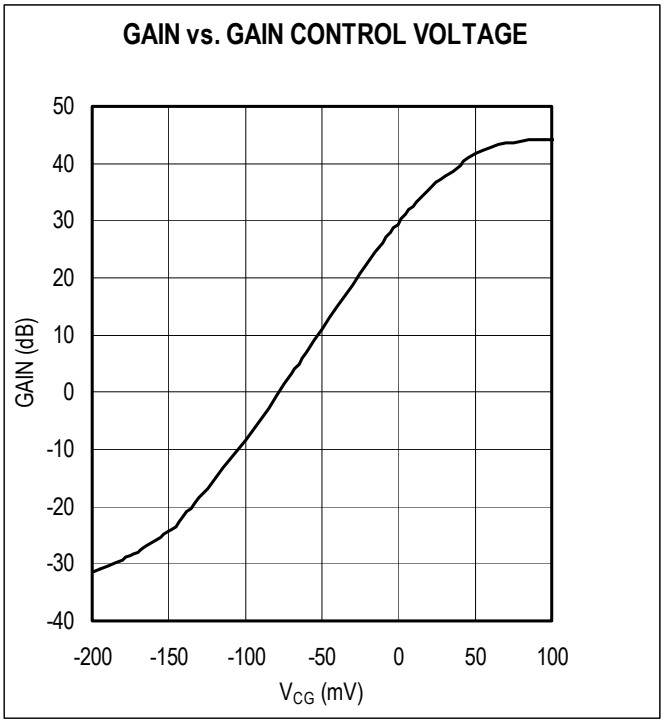

Figure 1. Gain vs gain control voltage (CG+ - CG-)

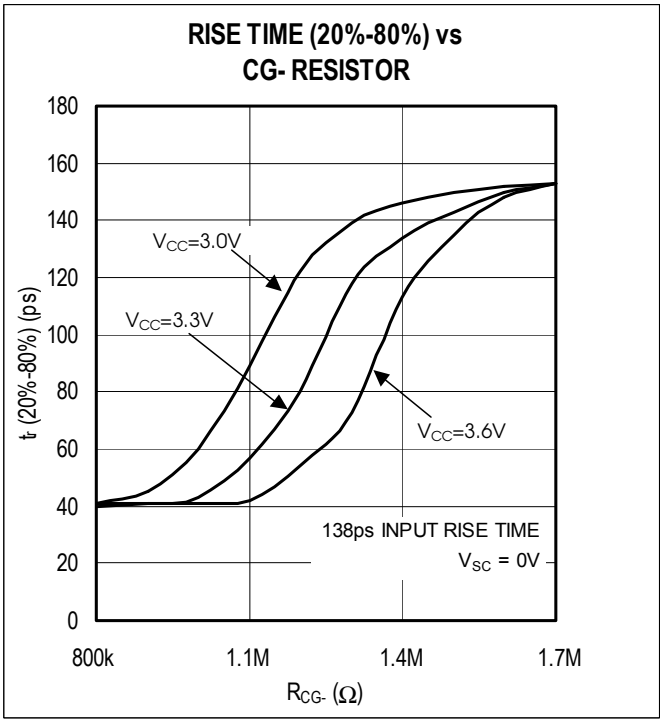

Figure 2. Data rise time vs CG- resistor (with 138ps input rise time)

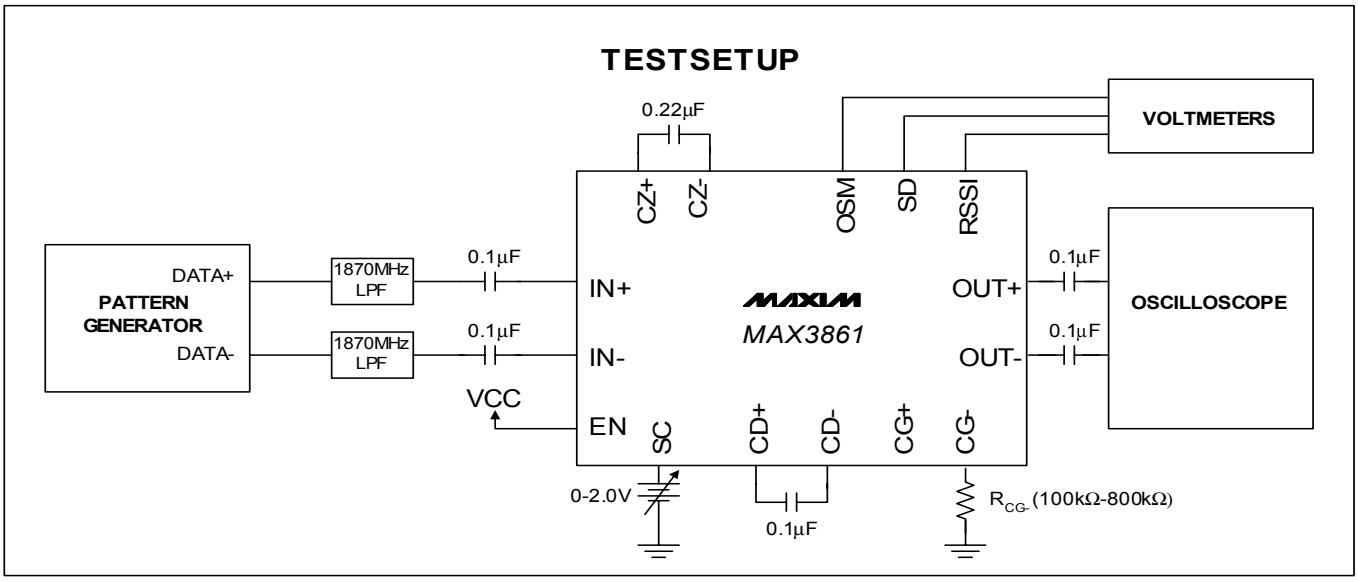

Figure 3. Test setup for the MAX3861

3.2 Component Count

The component count for limiting mode is the same as that for AGC mode because the gain control capacitor C_{CG}, described in the data sheet, can be eliminated. This capacitor closes the AGC loop, and is only necessary in AGC mode. By replacing capacitor C_{CG}, which connects across CG+ and CG-, with R_{CG-}, from CG- to ground, component count is kept constant.

4 Effects of Opening the Gain Control Loop

Aside from faster output edge speeds (Figure 4 and Figure 5) and greater tolerance to reflections on the input, there are a few additional effects from limiting mode.

4.1 Output Jitter

Overall, jitter decreases when the MAX3861 is limited. Deterministic jitter (DJ) remains approximately constant from AGC to limiting mode. Figure 6 illustrates this for V_{IN} = 6mV_{P-P} and V_{IN} = 20mV_{P-P}. In AGC mode at V_{IN} = 6mV_{P-P}, the DJ is 29ps_{P-P}. This is comparable to DJ in limited mode with R_{CG-} > 700kΩ. For V_{IN} = 20mV_{P-P} in AGC mode, DJ is 21.1ps_{P-P}, which is as high as the DJ reaches in limited mode.

The largest difference between limited and AGC mode is seen in the random jitter (RJ) output. With slow input edge speeds, a linear amplifier will produce a large amount of RJ, whereas a limiting amplifier will sharpen the edges and therefore decrease random jitter. As seen in Figure 7, RJ increases with increasing R_{CG-}, because the amplifier acts more like an AGC as R_{CG-} increases. Since RJ is decreased significantly, the total output jitter is greatly decreased when the MAX3861 is limited.

4.2 Output Amplitude

Since the gain is set to maximum and the internal amplifiers are therefore overdriven, the output amplitude will increase. This increase is about 25%, yielding an output amplitude range of 500-1150mV_{P-P} instead of 400-920mV_{P-P}.

4.3 Sensitivity

Just as in the AGC case, the SC pin controls the output amplitude. The only difference is that, since maximum gain is always being applied, the sensitivity will actually improve at lower output amplitudes. The sensitivity is still 6mV_{P-P} for an output of 920mV_{P-P}, but it improves proportionally as output amplitude decreases. It may be difficult to achieve an input sensitivity below 4mV_{P-P} in practice, though, because the signal will be in the vicinity of the noise floor.

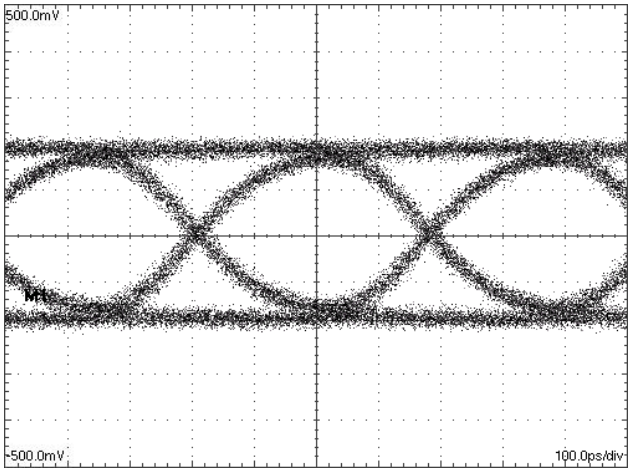

Figure 4. Output eye diagram in AGC mode (V_{CC}=3.3V, input edge speeds = 138ps)

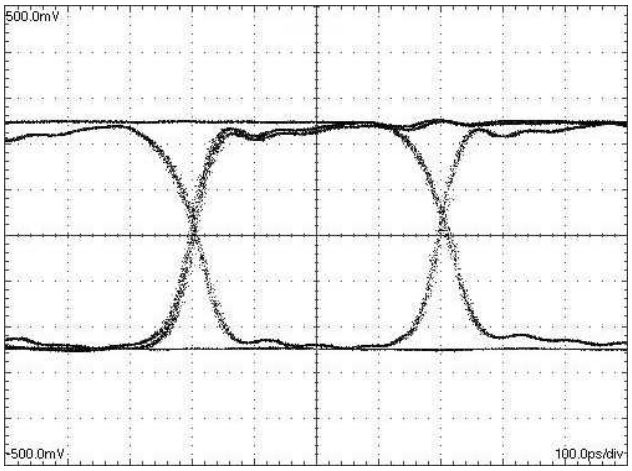

Figure 5. Limited eye diagram (R_{CG-}=1MΩ, V_{CC}=3.3V, input edge speeds = 138ps)

4.4 Unaffected Functions

Signal Detect, RSSI, and Output Signal Monitor are unaffected by operating in limiting mode rather than AGC mode. These all maintain normal operation over their specified operating conditions. From experimental data, the maximum V_{RSSI} difference between AGC mode and limiting mode at 25°C is less than 10mV.

In general, when put in limiting mode, the MAX3861 provides at least as good of performance as when in AGC mode.

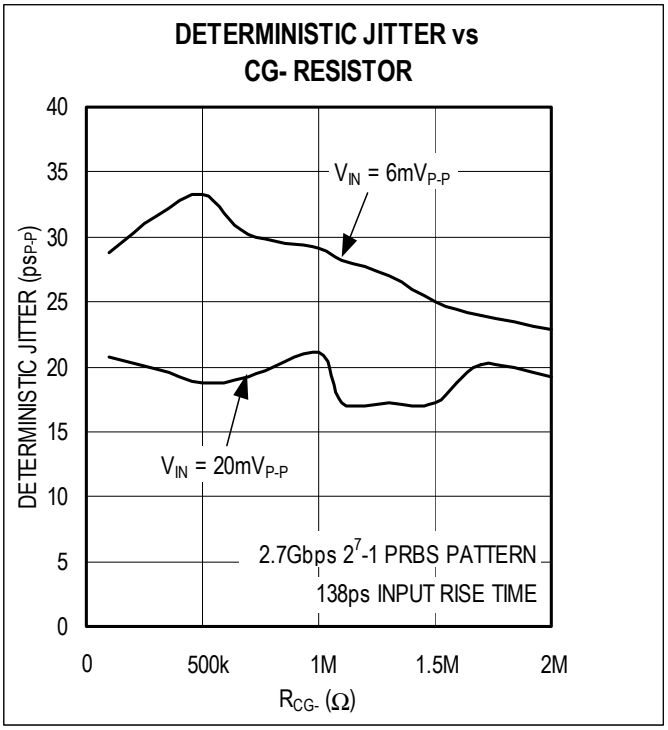

Figure 6. Deterministic jitter vs CG- resistor (with 138ps input rise time)

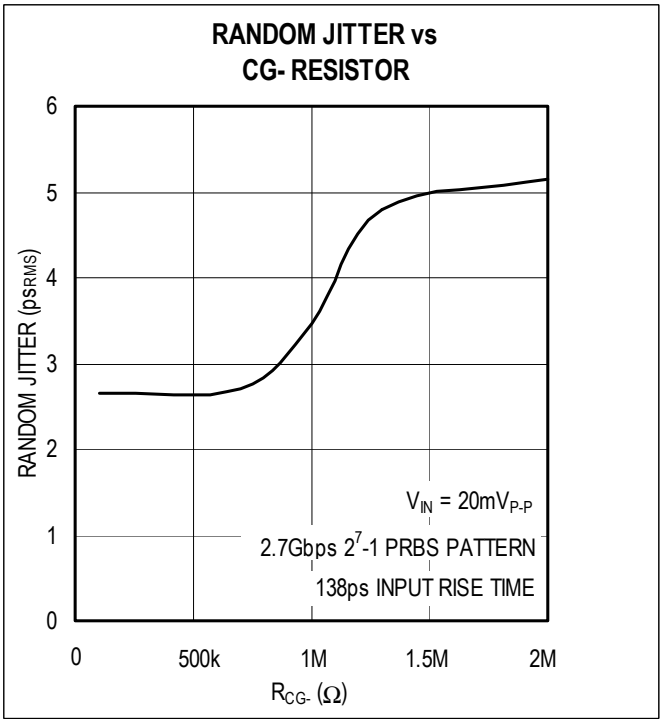

Figure 7. Random jitter vs CG- resistor (with 138ps input rise time)

5 Conclusion

The MAX3861 Automatic Gain Control Amplifier can easily be configured as a limiting amplifier, without degradation in performance or increased component count. With one simple modification, the MAX3861 becomes an ideal solution for SFP applications.